REMARKS

In the Office Action dated February 25, 2005, the Examiner rejected claims 1-8, 11-12 and 14-18 under 35 USC 102(e) as anticipated by Tsuji (U.S. Patent No. 6,255,740), rejected claims 9, 10, and 13 under 35 USC 103 as unpatentable over Tsuji and Wang (US Patent 6,258,626), and rejected claims 19-21 under 35 USC 103(a) as unpatentable over Lin (U. S. Patent 5,830,800). In response thereto, the Applicant has amended claims 19 and 20. Claims 1 through 21 remain at issue.

35 USC 102 Rejections

The Examiner rejected certain claims as anticipated by Tsuji. The Applicant strongly disagrees. Tsuji does not anticipate the present invention.

Figures 19A through 21C of Tsuji are the most relevant to the present invention. In each of these Figures, the active or conductive surface of the semiconductor chip is always facing upward. The non-active surface of the chip is facing downward.

In Figures 19A and 19B for example, wire bonds 43 are used to electrically couple contact pads 41a (not visible) on the top or active surface of the semiconductor chip 41 to connecting portions 52a formed on frame terminal 27. See specifically Column 17, lines 38-42.

Figures 21A-21C show the same arrangement as Figures 19A and 19B, but after the portions 66 between the terminal portions 28A of the frame terminal are removed. See Column 17, lines 43-59.

With the present invention, the claims clearly recite that the active or conductive side of the die faces downward and is positioned on the lead posts. Tsuji therefore does not anticipate the claims of the present invention. In fact, with the orientation of the die in the Tsuji reference actually opposite that of the present invention, Tsuji actually teaches away from the present invention. Claims 1-18 are therefore allowable.

The Applicant also strongly disagrees with the Examiner with regard to the Lin reference. The Examiner has misconstrued the actual teaching of this reference and has failed to demonstrate a prima facie case of obviousness.

Lin teaches a packaging method for ball grid array integrated circuits. The packaging method involves mounting a chip 40 with its active or non-conductive surface facing upward

onto a thin copper sheet 10. Gold wires or wire bonds 41 are used to electrically connect contact pads on the top surface of the chip to projections 30 on the copper sheet 10.

In contrast, the claims of the present invention recite a lead frame having a plurality of posts and a plurality of semiconductor die, each of the plurality of die having conductive pads mounted onto the plurality of posts of the lead frame respectively. The teaching of the Lin reference is therefore the opposite of the present invention. The orientation of the active surface of the chip of Lin is facing upward, whereas with the present invention, the orientation of the chip is facing downward with its conductive pads in contact with the posts of the lead frame. The Lin reference therefore actually teaches away from the present invention and does not teach or suggest the present invention. Claims 19-21 are therefore allowable.

It is respectfully submitted that all pending claims are allowable and that this case is now in condition for allowance. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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